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PATENT APPLICATION

UART AUTOMATIC HALF-DUPLEX DIRECTION CONTROL WITH PROGRAMMABLE DELAY

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UART AUTOMATIC HALF-DUPLEX DIRECTION CONTROL WITH PROGRAMMABLE DELAY

BACKGROUND OF THE INVENTION

The present invention relates to universal asynchronous receiver-transmitters (UARTs), and in particular to setting a delay between a last transmission and the reception of data.

UARTs are used in many communications applications to convert data streams from parallel to serial, enabling a serial data stream to communicate with a central processing unit or CPU. UARTs have increased in complexity over the years, with a single UART being able to serve multiple channels.

In operation, a typical FIFO will transmit data until its first-in, first-out (FIFO) transmit buffer is empty. It will then send a control signal indicating it is ready to receive data, the receive transmit signal (RTS). A complication that arises is that the data emptied from the buffer is shifted out onto the serial communication line via a shift register. In addition to the buffer being emptied, time must be allowed for the last word to shift through the shift register.

In addition, an amount of time must be allowed for the transmission time for the last word over the transmission line. This time can vary depending upon the length of the transmission line, its quality, the termination impedance, etc. Accordingly, most communication channels have a built-in delay which allows sufficient delay for a worst case of this combination of events. The delay is typically timed from the TxRDY signal, which is generated from the start bit of the last word. Thus, the delay is from this start bit. Even the word length can vary in some applications, thus this produces another variation in the amount of delay needed.

Some users have desired to customize their applications to shorten this delay where they know they have a short transmission line, good quality, etc. In one known embodiment, this is done by using a programmable logic array (PAL) connected on a board to the UART, with discreet resistors being used to set the delay time. The RTS signal is intercepted, delayed appropriately using the TxRDY signal, and then allowed to proceed after the delay (which is set by the external PAL circuit and discreet resistors). It would be desirable to simplify and improve the accuracy of such a programmable delay.

SUMMARY OF THE INVENTION

The present invention provides a UART with a FIFO buffer. A circuit detects a last word transmitted from the FIFO buffer. A transmitter empty circuit generates an internal transmitter empty signal when the last word transmitted from the FIFO buffer is detected. A delay circuit delays generation of the RTS signal for a programmable time delay from the transmitter empty signal. The time delay is set by a register that is programmable by the user. The invention thus provides the programmable delay on the same chip as the UART.

Preferably, the transmitter empty signal is an internal signal triggered from a stop bit of the last word, rather than the TxRDY signal generated from the start bit. Thus, this will automatically account for variations in word length.

Preferably, the programmable register is a shadow register which is a portion of a read only register used by the user and already in place on the UART. This eliminates the need for adding an additional register. In one embodiment, this is the first four bits of a modem status register.

In still another aspect of a preferred embodiment, the UART supports a plurality of channels. Preferably, at least eight channels are supported. Each channel will have its own FIFO transmit buffer and a circuit for detecting the last word and generating a RTS signal. The delay circuit is common to all of the channels, and can be shared among the multiple channels. Similarly, the programmable register is a single programmable register used for the delay for all the channels. In an alternate embodiment, each channel, or subgroups of channels could have their separate delay circuit and programmable delay so that a single UART could provide different delays depending upon the different channel transmission line characteristics, as determined by the user.

For a further understanding of the nature and advantages of the invention, reference should be made to the following description taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram of a UART incorporating the present invention.

Fig. 2 is a block diagram of the delay circuitry connected to one channel of the UART of Fig. 1.

Fig. 3 is a timing diagram illustrating the delay timing in an embodiment of the invention.

Fig. 4 is a block diagram of the programmable delay register as a shadow register is one embodiment of the invention.

DESCRIPTION OF THE SPECIFIC EMBODIMENTS

Fig. 1 is a block diagram of a UART 10. The UART includes eight channels 12. Channel 0 indicates the internal circuitry for that channel, which is not shown but would be the same for the other eight channels. In particular, it has a 64-bit transmit first in/first out (FIFO) buffer 14 and a 64-byte receive FIFO 16. The channel also includes other control circuitry and registers. The channels interface via I/O lines 18 to serial data communication lines. The data can be provided through an internal bus 20 to an internal FIFO manager 22. The FIFO manager provides the data in both directions through a second internal bus 24 to a PCI local bus interface 26. This interfaces with a PCI bus 28.

Directly accessible by the PCI local bus interface 26 are a series of device configuration registers 30.

Fig. 2 is an embodiment of the delay circuitry of the invention for one of the channels of Fig. 1. A transmit FIFO 14 is shown, with the transmitted bits being transmitted through a shift register 40 to the transmit pin (TXO) 42 of the UART. A transmit ready signal (TXRDY) on a pin 44 is generated from the last word in FIFO 14, from the start bit of the word. The present invention adds a stop bit detector circuit 46 which detects the last word from FIFO 14 and also detects the stop bit from shift register 40. When the stop bit is detected, it is provided to a programmable counter 48. The programmable counter counts down the amount of time as set by programmable register 50, which stores the user set programmable delay. When this count is reached, a signal is provided through a buffer 52 to RTS pin 54.

For multiple channels, the programmable register is shared, but the rest of the circuitry is duplicated in each of the channels.

Fig. 3 illustrates the timing of the invention. A last word 56 is illustrated having a start bit 58 and a stop bit 60. In existing UARTs, the TXRDY signal is generated from start bit 58. Since the length of last word 56 can vary, existing systems need to account for this possible variation in word length and have the delay appropriately some time after that maximum word length. The present invention, on the other hand,

generates a signal which is triggered off the stop bit 60. This signal, designated herein as a transmitter empty signal, is generated at a point 62. The delay circuitry shown in Fig. 2 will delay this until a point 64, with the delay being programmable by the user.

Fig. 4 shows an embodiment of the programmable delay register 50 of Fig. 2 as a delay shadow register. The shadow register is a shadow register to the modem status register 64. As a shadow register, the same address lines 66 address both registers at the same register address. However, the data lines 68 are configured to be read from register 64 through a buffer 70 in response to a read signal. However, a write signal provides the data to shadow register 50 through a buffer 72. Thus, the address space which is only used for reading purposes by the user can also serve, in response to a write by the user, to set the delay. The user does not need to read back the delay signal, so it is simply used as an output internally to the programmable counter of Fig. 2.

The present invention thus allows the user to account for variations in the word length in the FIFO buffer. This word length can vary, for instance, from 7-12 bits in some embodiments. In addition, the user can programmably set the amount of delay appropriate for the particular configuration used by the user. This configuration may vary depending upon the length of the transmission line, the quality of the transmission line, the quality of the termination impedance, the noise environment affecting the signal quality, etc.

As will be understood by those of skill in the art, the present invention can be embodied in other specific forms without departing from the essential characteristics thereof. For example, instead of the delay register and circuitry being shared by multiple channels, a separate delay circuit and register could be used for each subset of four channels. Alternately, each channel could have its own delay register in an alternate embodiment. In addition, alternate register locations could be used. Accordingly, the foregoing description is intended to be illustrative, but not limiting, of the scope of the invention which is set forth in the following claims.